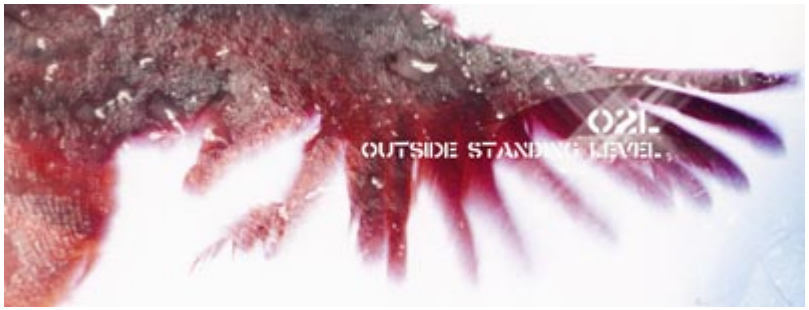
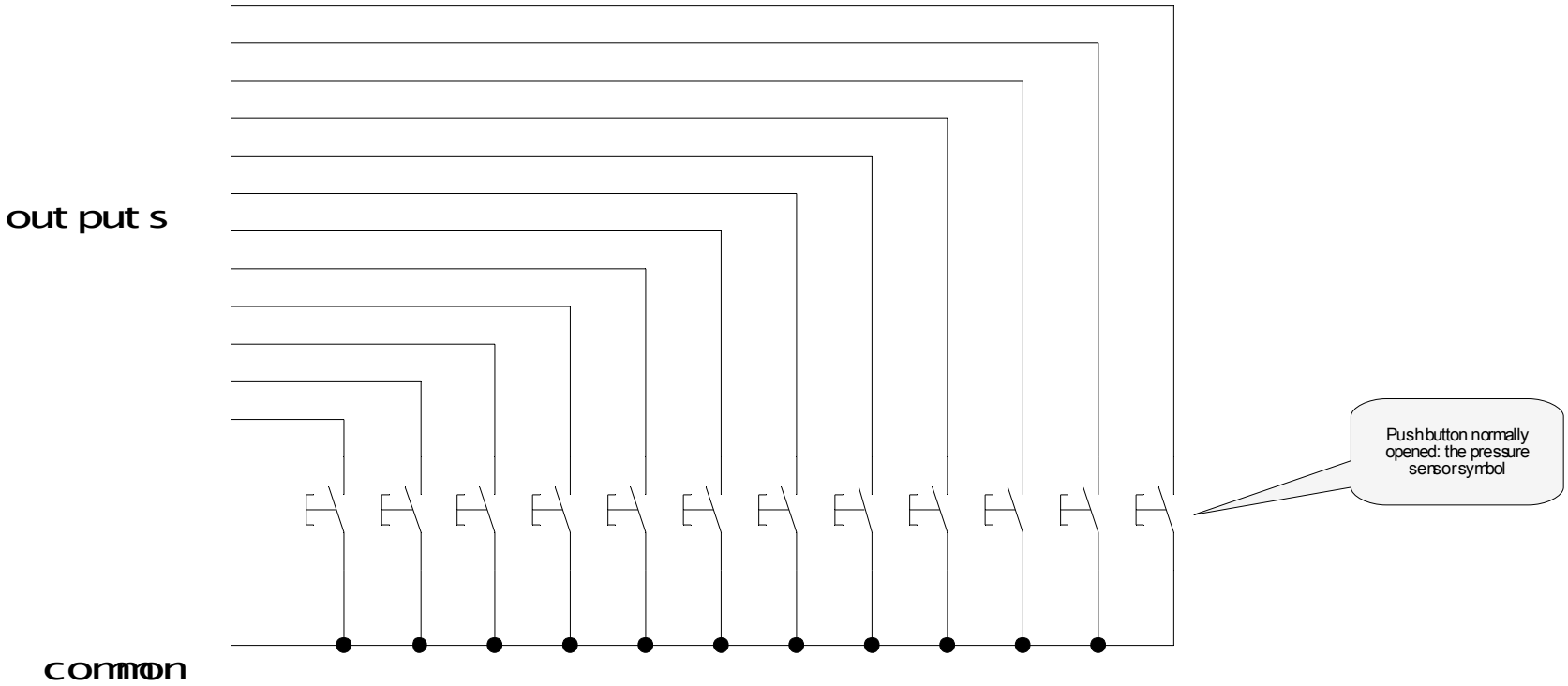


Scala Infinita 2.0

wiring: technical drafts

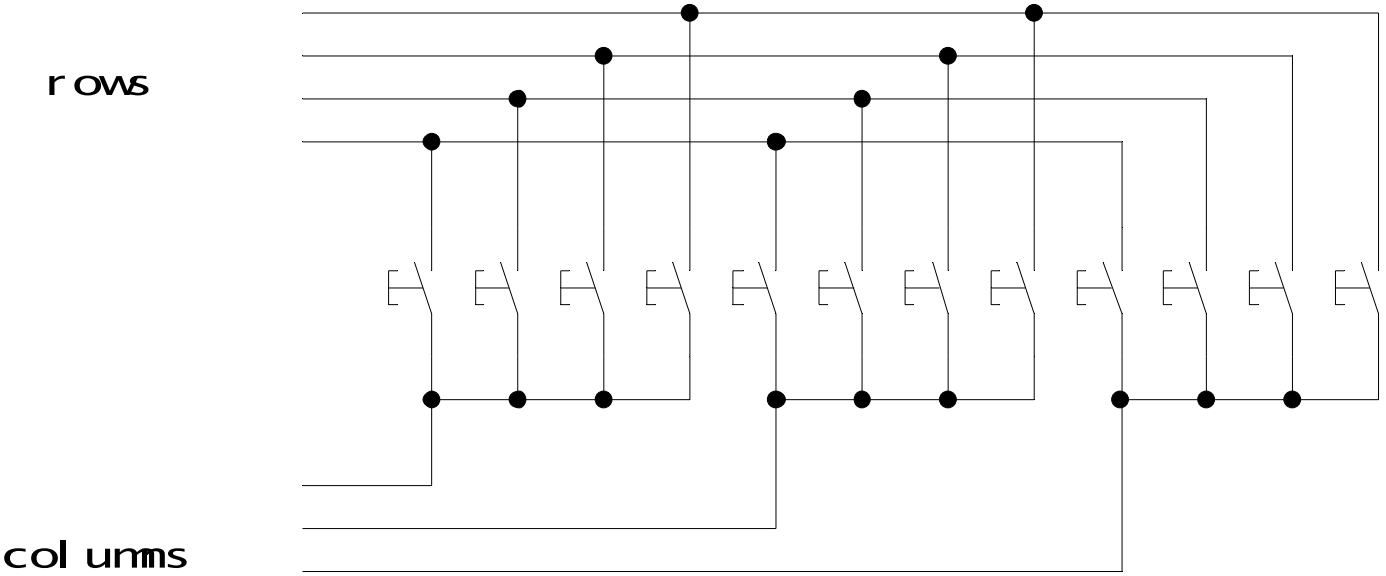
This is the simplest way to connect 12 sensors.
Simplicity is intended at detection level, not at deployment phase: this method requires 13 wires, which are quite several to be routed.
The main advantage is the unsimulated parallel detection: there's no delay between reads, which happen at once.

The first version of SI is based on this topology, due to the needs of making each syntesis module perfectly independent. Routing was quite critical on the collector (where all the wires join).



Wiring topology: parallel version schematics

This is a common way of save pinouts making a combinatoric arrangement of the connections (in fact there are 5 wires less of the full parallel version, this is what we can call a 'shared bus topology').
This way has the unpairable advantage of permitting a 8-bit port to fullfill the mapping needs of the sensor array.
However, even if the bus-topology develops indeed a more conservative and compact design, leads also to a growt complexity of the detection mechanism.
Columns are scanned sequentially and rows are read at specific time.
Scan time could be very small and substantially undetectable by the user.



Wiring topology: bus version schematics

row 1

row 2

row 3

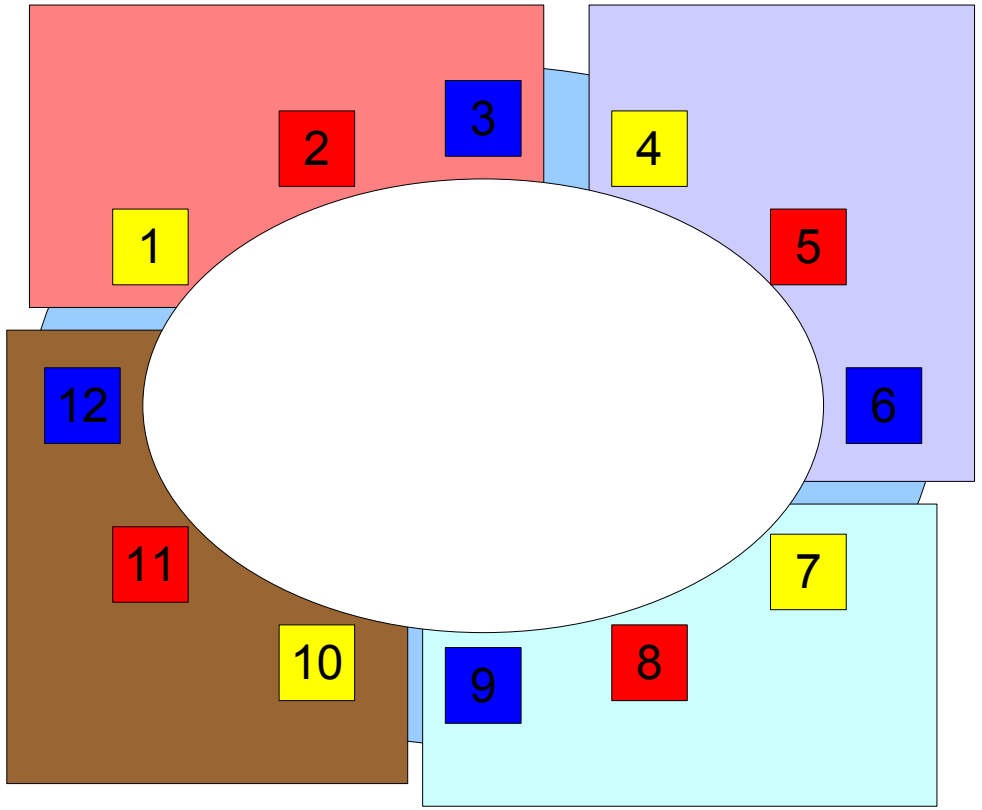
row 4

column A

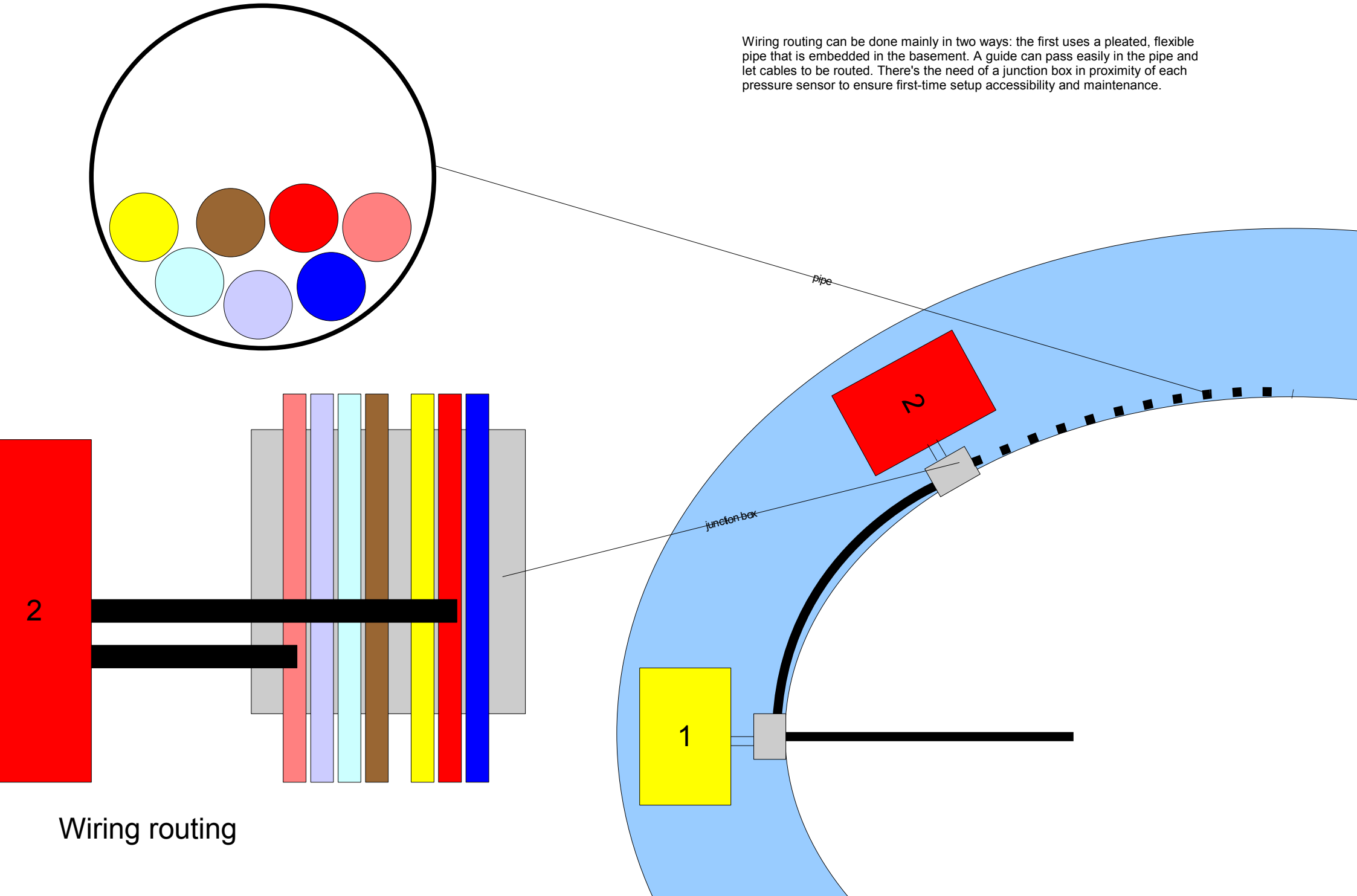
column B

column C

This page shows the disposition of the pressure sensors, related to the columns/row logic.
Refer to the page 3 schematics to get a better overview of the wiring scheme.



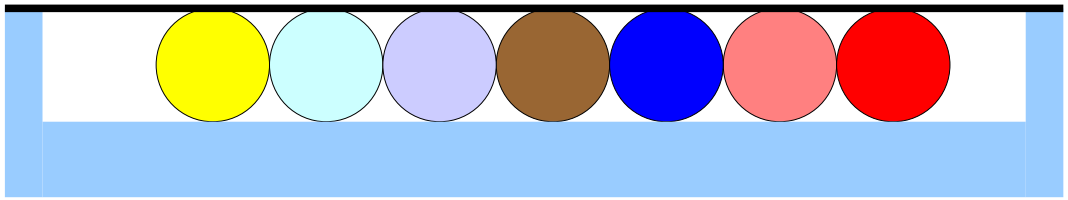
Wiring topology: bus version blocks

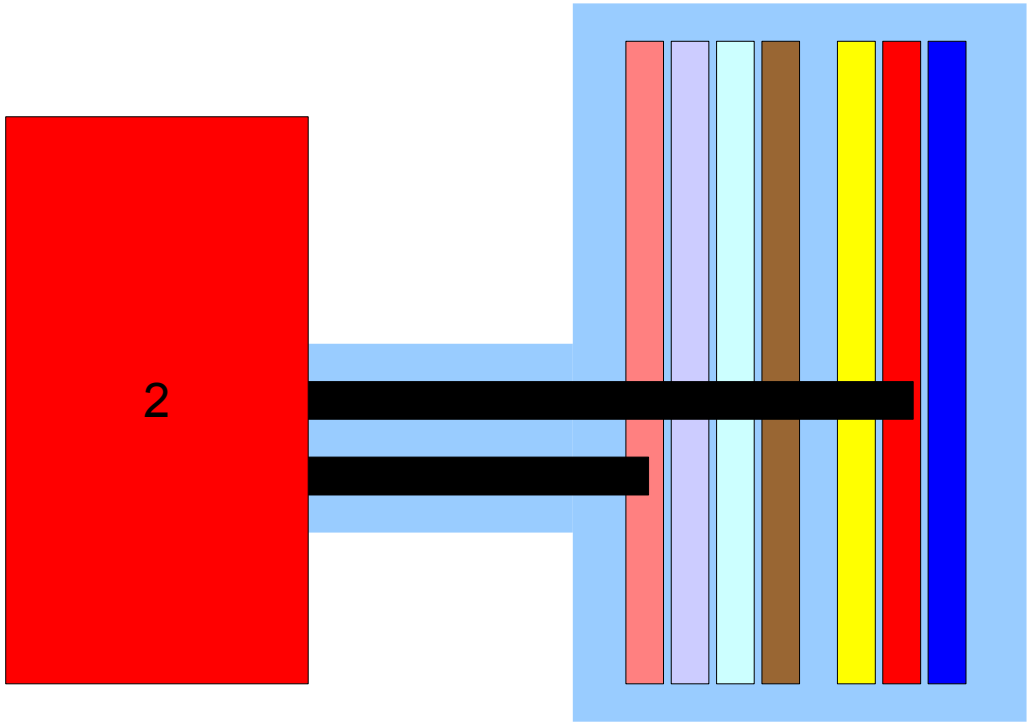


Wiring routing can be done mainly in two ways: the first uses a pleated, flexible pipe that is embedded in the basement. A guide can pass easily in the pipe and let cables to be routed. There's the need of a junction box in proximity of each pressure sensor to ensure first-time setup accessibility and maintenance.

Wiring routing

Second way uses a groove in the basement where cables can be embedded. Routes to the sensors are made by intersection grooves. Junctions are low profile terminal blocks.





Wiring routing

Basing on the first version of SI, maximum running length (including collector stub) can be approx. 20m. Therefore signal loss due to resistance is trascurable.
Cables can be as small as AWG 30 (expecially on the prototype, where clutter is a key feature), mono core (solid) or multi-core/stranded.
However, a good solution is AWG 24 taken off from a cat.5 UTP cable (even if, being a solid conductor is quite unflexible).

SI ver.1 has been deployed with AWG 23 multi-core cables, using crimp sockets to interface cables to PCBs.

Wiring notes